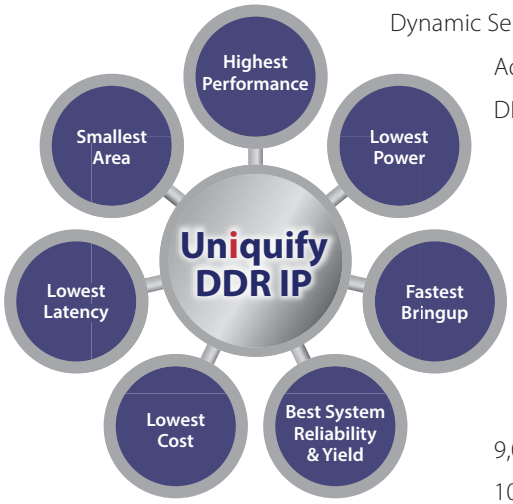
DDR Revolution

World's Fastest, Smallest, Lowest Power DDR Subsystem IP

Uniquify's innovative adaptive DDR memory subsystem IP enables customers to achieve the fastest, smallest, and lowest power DDR performance giving them a key competitive edge.

Complete DDR IP Subsystem Solution

The DDR memory subsystem (DDR controller, PHY and IO) is critical to the successful operation of a SoC. System performance and field reliability demand that the DDR subsystem implementation offer the highest performance while at the same time offering the highest quality, in combination with a small footprint and minimal power consumption. Uniquify offers a complete set of silicon-proven IP for implementing DDR4/3 and LPDDR4/3/2 subsystems in 22/28/40/55nm processes, including 14nm FinFET and 22nm FD-SOI from multiple foundries. Uniquify's patented Self-Calibrating logic (SCL), Dynamic Self-Calibrating Logic (DSCL), Adaptive Bit Calibration (ABC), and Dynamic Adaptive Bit Calibration Logic (DABC) technologies automatically adjusts the DDR interface timing at power up and dynamically during system operation to mitigate both static and dynamic variations. This allows each system to achieve the highest possible DDR performance with the smallest area and lowest power without sacrificing reliability. The SCL, DSCL, ABC, and DABC technologies are covered by 18 U.S. patents and are embedded within Uniquify's DDR PHY and operate seamlessly. Uniquify's DDR PHY (including SCL, DSCL, ABC, and DABC) utilizes the technologies protected by US Patents 7,975,164 8,661,285 8,843,778 8,990,607 9,021,293 9,081,516 9,075,543 9,552,853 9,300,443 9,584 309 9,431,091 9,805,784 10,229,729 10,032,502 10,242,730 10,269,408. Additional patents may be pending in the U.S. and elsewhere. No other DDR IP on the market offers this breakthrough technology.



Uniquify™

Key DDR Subsystem Features

DDR Controller

- Highly flexible and customizable DFI 4.0 compliant DDR controller architecture
- Supports up to 32 independent target interfaces including AXI, AHB and FIFO-based interfaces
- User-customizable arbiter (scheduler)

DDR PHY

- High performance, small footprint DFI 4.0 compliant PHYs—DDR4,3 and LPDDR4,3,2
- Low power operation
- Supports LPDDR4 at 4.2Gbps and DDR4 at 3.2Gbps and DDR3/LPDDR3 at 2.133 Gbps
- Built-in SCL and ABC circuitry for highest performance, low power operation and field reliability
- Flexible implementation and customization support—rectilinear layouts
- Many combination options for "combo" PHYs that support multiple DDR protocols such as LPDDR4/LPDDR3, LPDDR3/LPDDR2, DDR4/LPDDR3 and DDR4/DDR3

DDR I/O

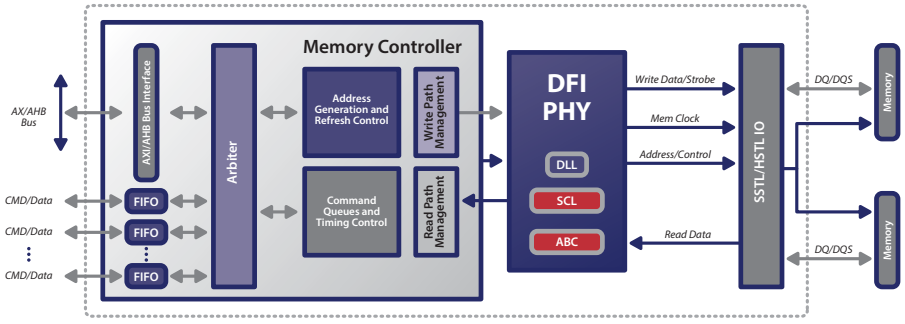
- High performance, low jitter DDR IO
- Low power / compact footprint
- Silicon proven

DDR Controller

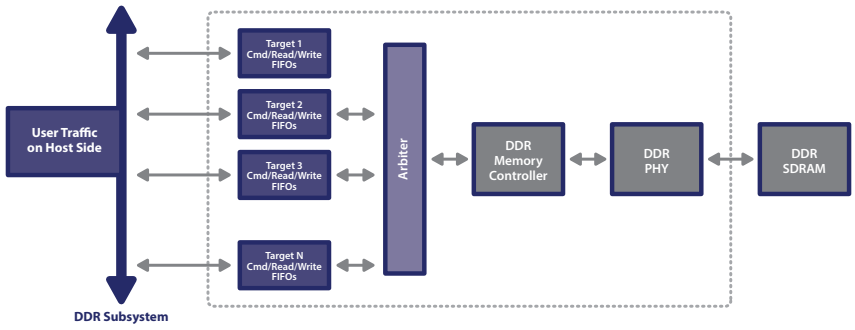
Uniquify's DFI 4.0 compatible DDR Controller provides a simple and flexible interface for accessing external DDR SDRAM memory. It provides advanced power saving features such as automatic entry into active power down, pre-charge power down, and self-refresh operations. It achieves high performance through maximum utilization of multiple open banks and command look ahead.

The DDR Controller can operate at half the clock frequency as the SDRAM memory (half-rate mode).

The Controller comes configured with one or more independent "targets" based on the design requirements needs—from 1 to 32 or even larger as required. Supported targets include AXI, AHB and a custom FIFO-based target interface. Each one supports flexible customizations such as data path width, transfer length, read and writes data buffering and byte enable support. Verilog testbench tasks and C routines that perform controller initialization and SDRAM initialization are provided to simplify integration of the IP and interface bring-up. The Controller includes a very flexible arbiter that shares access to the Controller across all of the targets. Many different schemes can be implemented including minimum number of consecutive accesses, minimum bandwidth, bandwidth optimization, prioritization based on request, and many others.



DDR Subsystem IP Diagram



DDR System Block Diagram

DFI 4.0 Compatible PHY

The leading edge DDR PHY IP, innovated and designed by Uniquify is production proven in silicon. By combining a DFI 4.0 compatible PHY interface with patented SCL and ABC circuity, the Uniquify PHY offers the following key benefits:

- Highest possible DDR performance
- Smallest footprint available
- Highly flexible, rectilinear PHY layouts
- Lowest power
- Lowest latency
- Automated, faster DDR bringup
- Best system reliability and improved yield
- Simplified operation via register programming
- DFI 4.0 compatibility with backward compatibility to earlier DFI standards for ease of integration with DFI-compliant DDR controllers

Uniquify offers PHY solutions for DDR4/3 and LPDDR4/3/2 with speeds up to 4.2Gbps and silicon-proven solutions at a wide variety of process nodes from 55nm through 14nm. Each PHY is delivered as a hardened block optimized to drop directly into the target SoC. When coupled with Uniquify's DDR IO IP, the combined solution eliminates tough timing problems such as data/clock skew, setup/hold time and complex physical implementation issues.

Trim Value

	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8
L0B0	2	2	3	3	3	3	3	3	3	3	3	2	2	2	2	2	2
L0B1	2	2	2	3	3	3	3	3	3	3	3	3	2	2	2	2	2
L0B2	2	2	2	2	3	3	3	3	3	3	3	3	2	2	2	2	2
L0B3	2	2	2	2	3	3	3	3	3	3	3	3	3	2	2	2	2
L0B4	2	2	2	2	3	3	3	3	3	3	3	3	2	2	2	2	2
L0B5	2	2	2	3	3	3	3	3	3	3	3	3	2	2	2	2	2
L0B6	2	2	2	2	3	3	3	3	3	3	3	3	3	2	2	2	2
L0B7	2	2	2	2	3	3	3	3	3	3	3	3	3	2	2	2	2
L1B0	1	1	3	3	3	3	3	3	3	3	3	1	1	1	1	1	1
L1B1	1	1	1	3	3	3	3	3	3	3	3	1	1	1	1	1	1
L1B2	1	1	1	3	3	3	3	3	3	3	3	1	1	1	1	1	1
L1B3	1	1	1	3	3	3	3	3	3	3	3	3	1	1	1	1	1
L1B4	1	1	1	3	3	3	3	3	3	3	3	3	1	1	1	1	1
L1B5	1	1	1	3	3	3	3	3	3	3	3	3	1	1	1	1	1
L1B6	1	1	3	3	3	3	3	3	3	3	3	1	1	1	1	1	1
L1B7	1	1	1	3	3	3	3	3	3	3	3	3	1	1	1	1	1

L0B0 = Lane 0, Bit 0

L1B0 = Lane 1, Bit 0

3 = Both lanes passing

2 = Only lane 0 is passing

1 = Only lane 1 is passing

Byte Lane/ Bit Alignment Provided by SCL and Adaptive Bit Calibration

Only From Uniquify: Self-Calibrating Logic Technology

The Uniquify PHY incorporates adaptive patented Self Calibrating Logic (SCL)) technology that automatically calibrates the DDR interface at power up and dynamically during system operation by centering the capture point in the middle of the timing window. Field-proven, SCL mitigates both static and dynamic variations in a system resulting in optimal DDR performance, improved device and system yield. SCL automatically solves the clock domain crossing problem and by eliminating much of the conventional overhead circuitry required for synchronization results in a smaller, more compact, lower power PHY. The operation of SCL is completely user-controllable

Read data capture timing and write alignment timing are setup automatically using SCL and at initialization and is periodically re-run every few seconds (or as specified by the user) in incremental calibration mode. All setup and control of the SCL is accomplished using register reads and writes and manual operation is also supported.

Adaptive Bit Calibration Technology

Uniquify's differentiator is its patented Adaptive Bit Calibration (ABC) technology. Like SCL, Adaptive Bit Calibration can also be run both at system startup as well as dynamically during system operation.

ABC automatically corrects for bit-bit skew and jitter within each byte lane. This provides for a more robust system and allows optimal performance to be achieved for a given board SDRAM even when using low-cost wire bond packaging.

Uniquify PHY Benefits

- Custom PHY hardened and delivered as GDS for ease of integration into host SoC
- Flexible, rectilinear layout options minimize footprint
- System bring-up time drastically reduced via SCL technology
- Patented dynamic ABC technology minimizes intra byte-lane skew for improved DDR system performance
- Enhanced ATE testability via SCL—traditional loopback testing also supported
- Industry-leading low read-data capture latency and command output latency
- Supports DFI clock disable feature for power savings
- SDRAM interface widths from 16-bits to 144-bits with flexible byte lane and command/address bus configurations

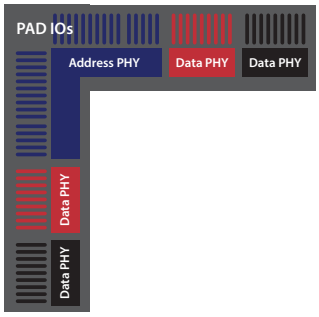
Uniquify™

High Performance DDR IO

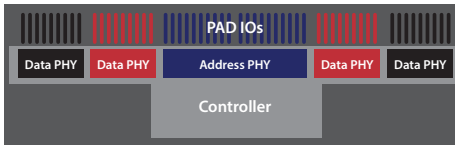
Uniquify provides a family of high performance, low power, low jitter JEDEC compliant DDR IO for DDR4/3 and LPDDR4/3/2 SDRAM systems. A wide range of drive strengths and terminations settings are provided per JEDEC standards as needed to accommodate multiple DDR standards and implementations.

Summary of DDR IO Features

- High speed, low jitter design for reliable operation
- Low power operation
- Compact footprint
- Wide range of drive strengths and termination settings
- Dynamic calibration of on-die termination and output impedance
- Robust ESD architecture



Compact, Flexible PHY Layout Options



Fully Hardened DDR Subsystem with Controller, PHY and IO

Production Proven Silicon Nodes

The DDR controller is delivered as RTL while the PHY and IO are delivered as hardened macros to fit the target chip floorplan and padframe. Uniquify can also deliver a fully hardened DDR subsystem (controller, PHY and IO) to minimize critical path timing iterations. For DDR subsystem testing, a comprehensive simulation testbench is provided.

PHY Deliverables

Verilog netlist, SPEF, LEF, LIB, timing reports, technical documentation, CDL netlist and clean GDSII.

IO DELIVERABLES

All PHY deliverables plus SPICE models and padframe guidance and review.

Technical Guidance

Uniquify provides complete layout and integration guidelines for the DDR IP and a technical review of the DDR subsystem implementation prior to tapeout. Support is also available for silicon bring up.

Foundry	Production Proven Silicon Nodes
GF	55LPe, 40LP, 28SLP/HPP, 22FDX
ICF	14FF
Samsung	28LPP
SMIC	55LL, 40LL, 28HK
TSMC	40G/LP, 28HPC/HPC+/HPM
UMC	28HLP

DDR Interface IP Supported on a Wide Range of Foundry Processes

Feature	Uniquify DDR IP	Competition
Power-Up Calibration	Performed by patented Self-Calibrating Logic (SCL)	Gate training per DFI standard
On-the-Fly Calibration	Performed by dynamic SCL	Not available
Calibration Range	+/- 4 clock cycles using patented technology	+/- ½ clock cycle
Per-byte lane training	SCL calibrates every byte lane independently, can accommodate wider skew (+/-4 cycles) across byte lanes	Limited to forcing tighter skew requirements
Read Latency	Under 3 clocks	5 or more clocks
Customization	PHY optimized to pad frame for area and performance	Off-the-shelf hard PHY requires buffer and delay matching in layout
Performance	Maximum data rate in mature silicon nodes, 30% faster that competition due to patented technology	Forced to use higher-power or smaller silicon for same data rate as Uniquify
Area	20-30% smaller in same silicon node: PHY alongside IOs, 50% shorter Pad frame, no FIFO logic	Needs buffers and routing to connect PHY to IOs, employs FIFO logic
Power	30-50% savings from better design, gated delay logic, clock gating, custom clock network, retention mode	Uses FIFO logic, no custom compiler
Field Reliability	Dynamic SCL compensates for component drift in the field	No compensation for component drift

Uniquify

2030 Fortune Dr., Suite 200

San Jose, CA 95131

Phone: 408-235-8810

DDR_Info@Uniquify.com